

FIG. 1

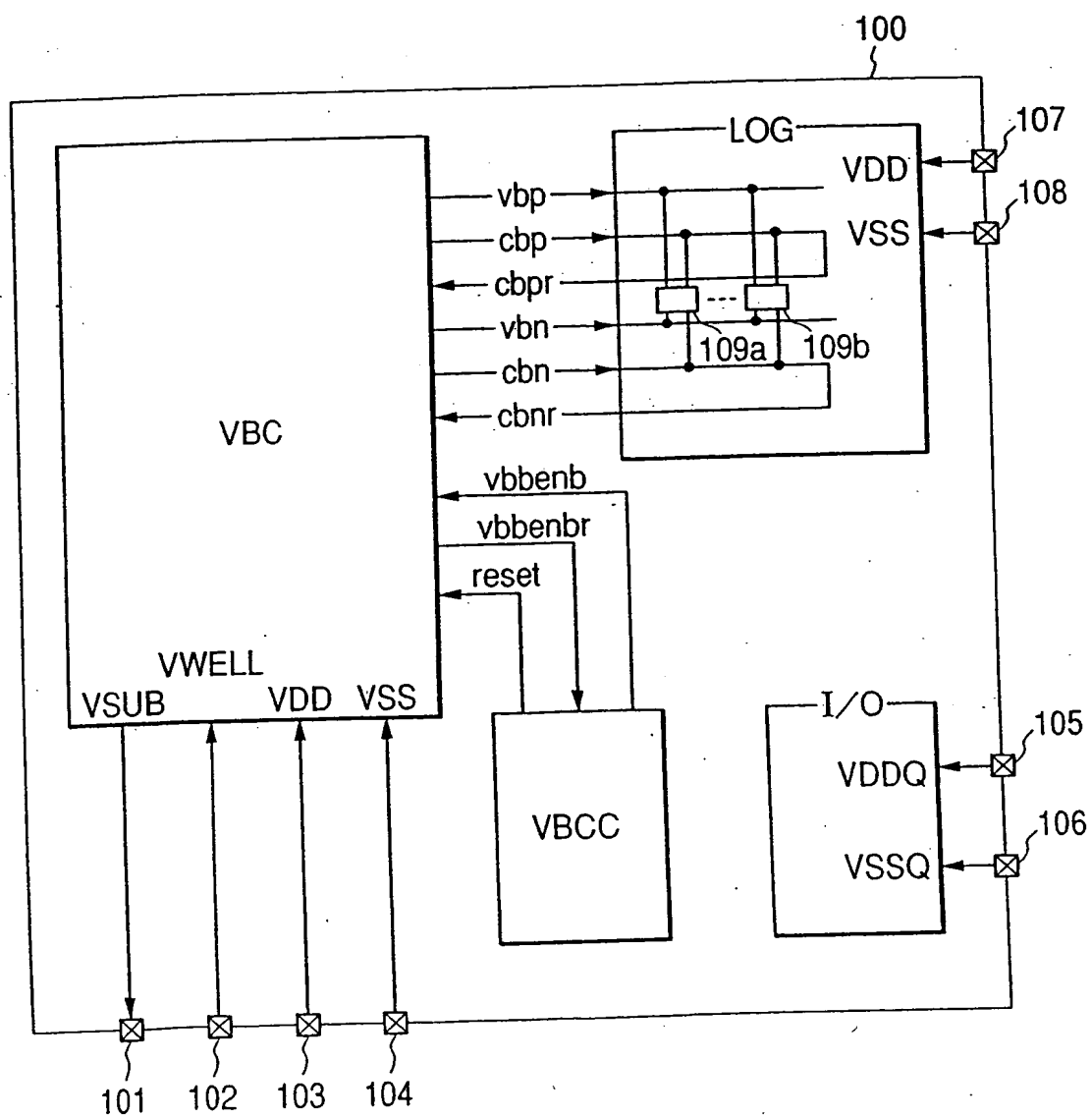


FIG. 2

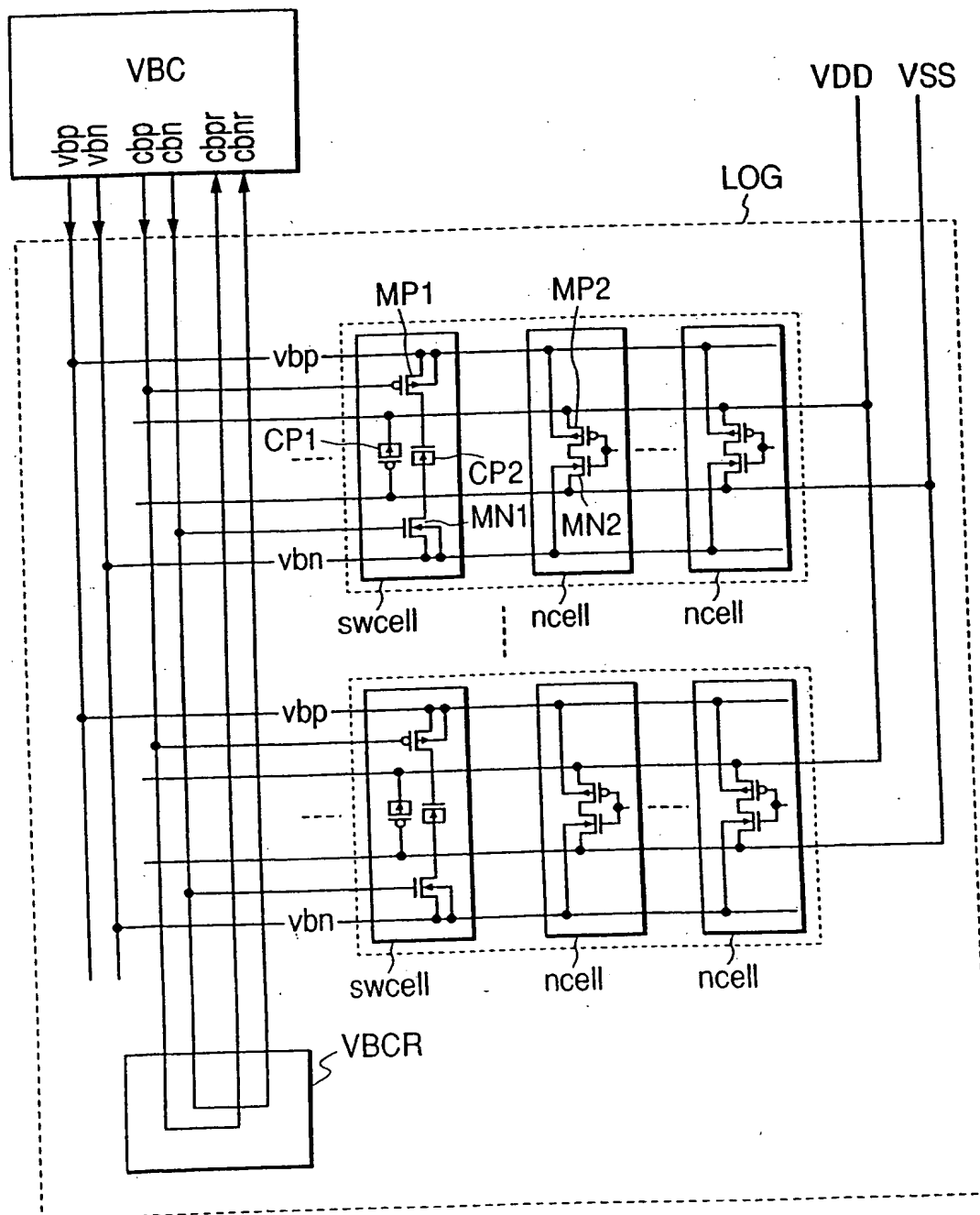
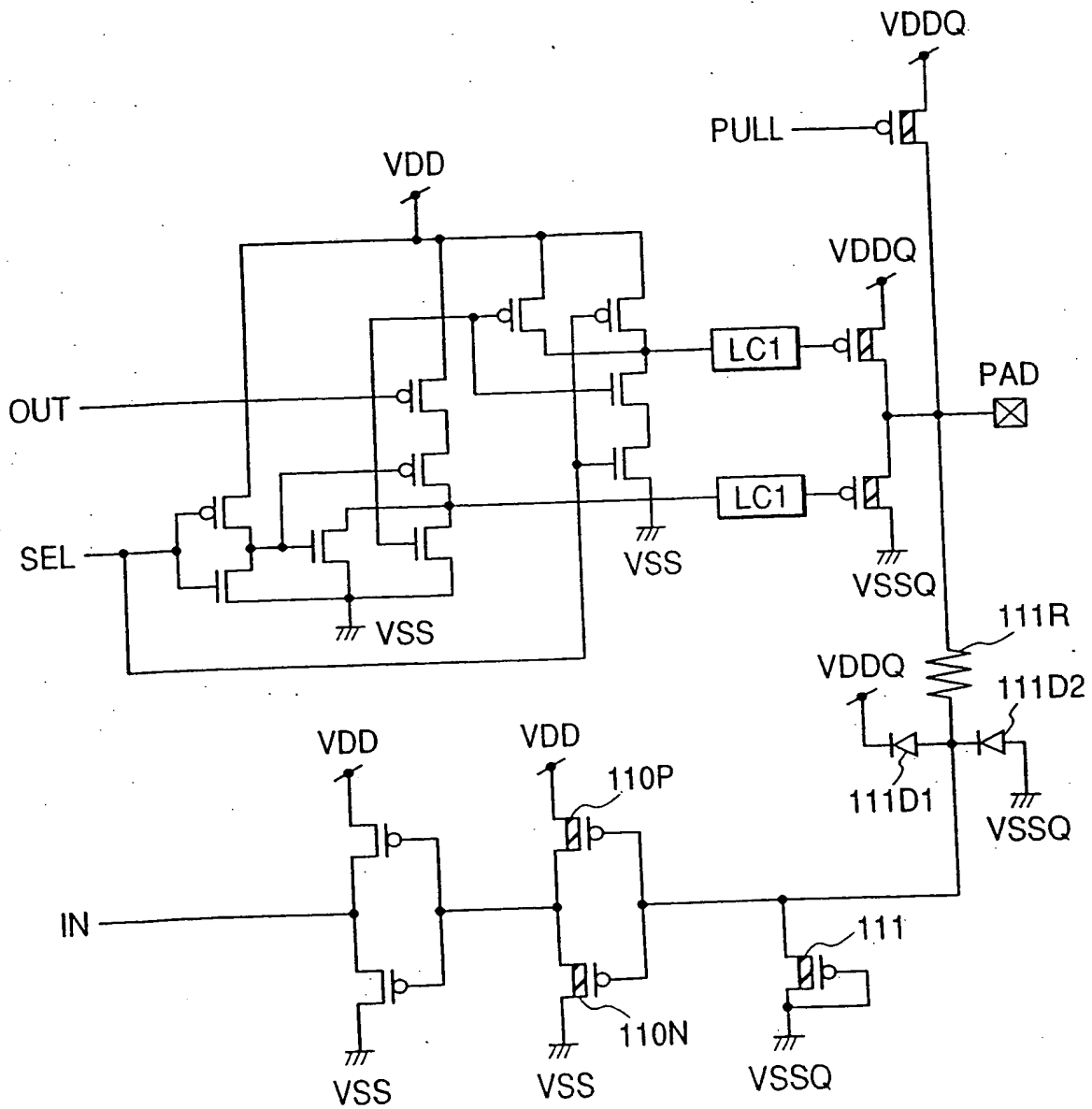
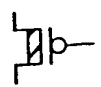



FIG. 3



  = THICK OXIDIZATION FILM TRANSISTOR, HIGH THRESHOLD LEVEL, WITHOUT V_{BB} CONTROL

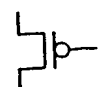

  = THIN OXIDIZATION FILM TRANSISTOR, LOW THRESHOLD LEVEL, WITH V_{BB} CONTROL

FIG. 4

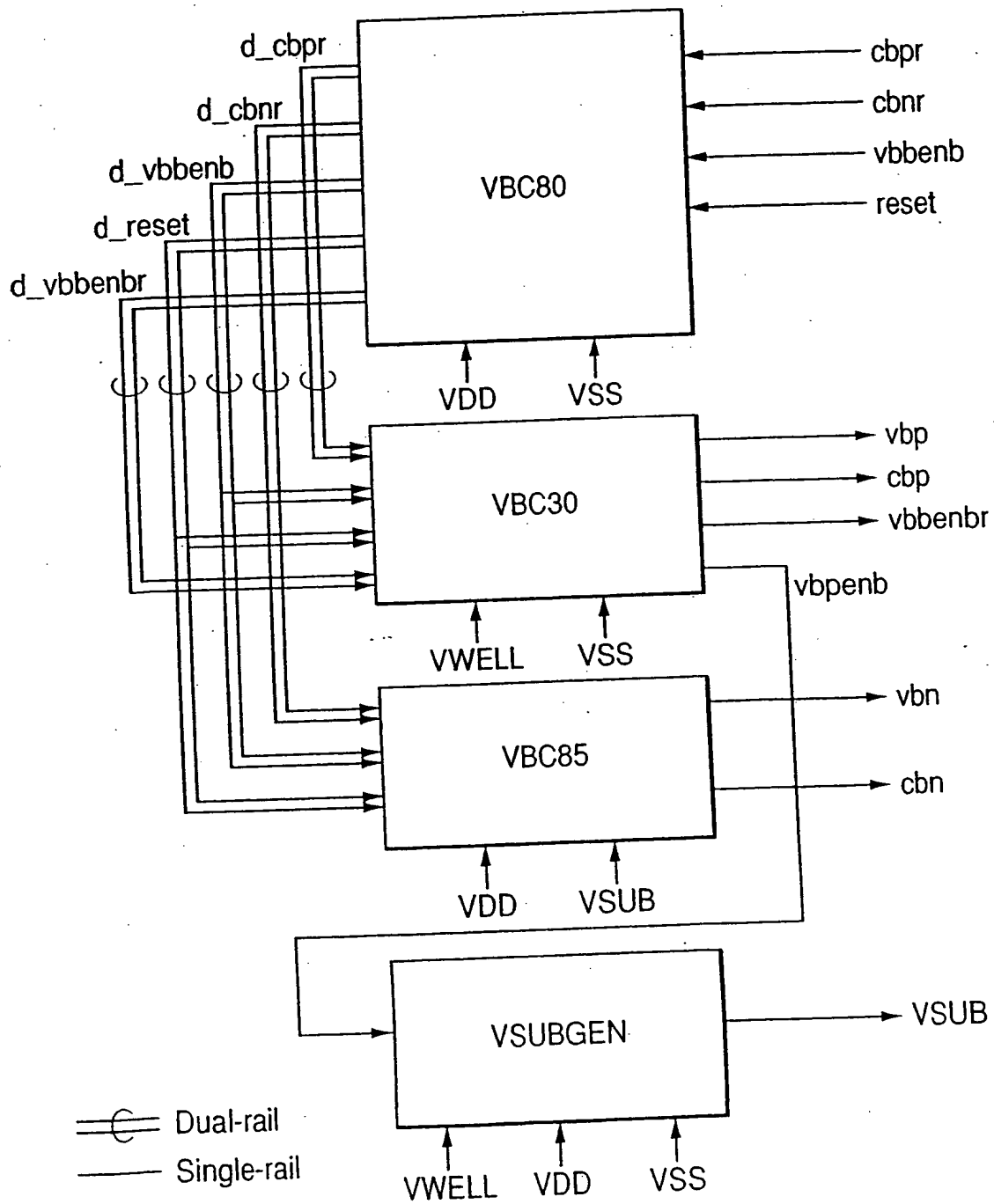
VBC

FIG. 5

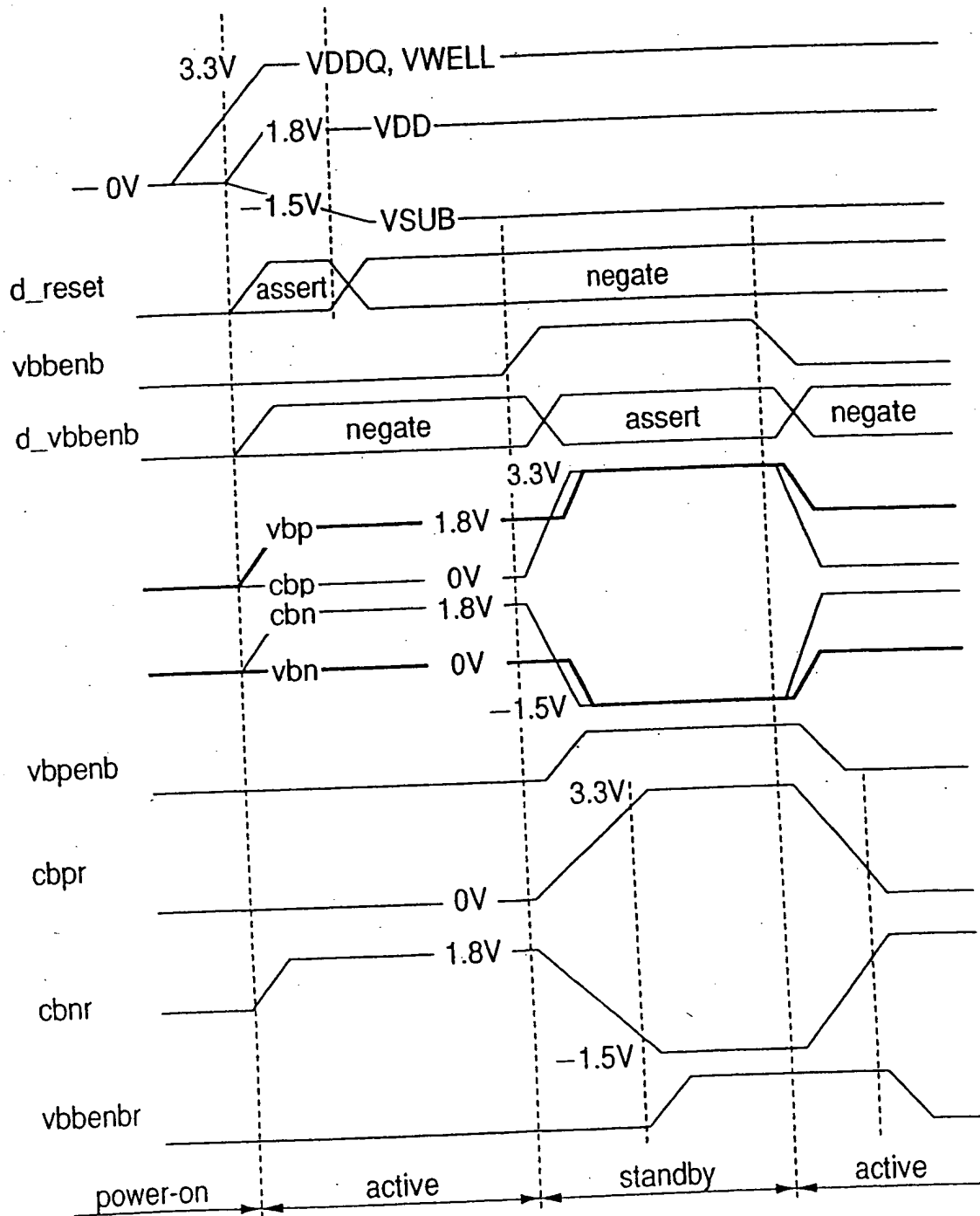


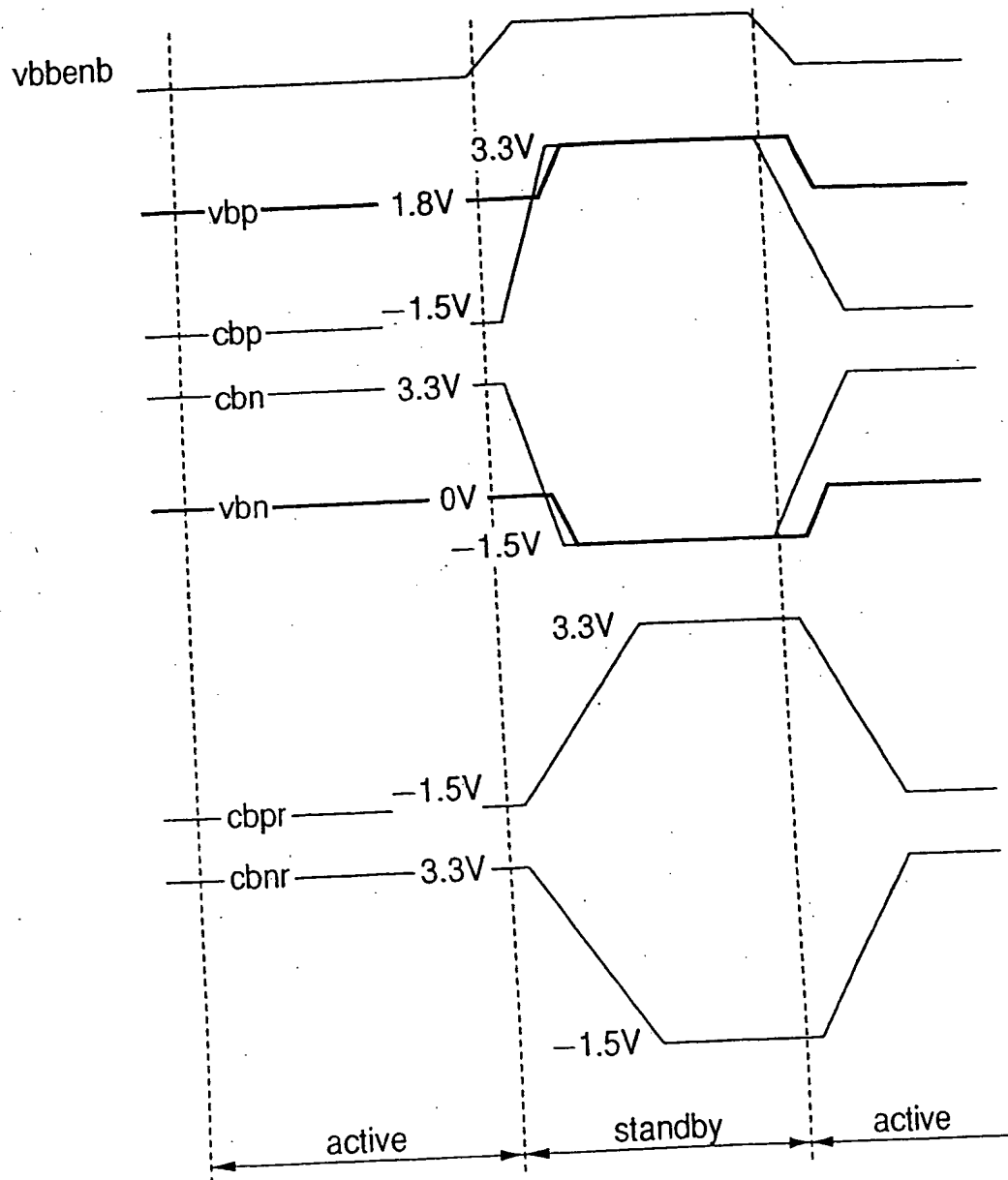
FIG. 6

FIG. 7

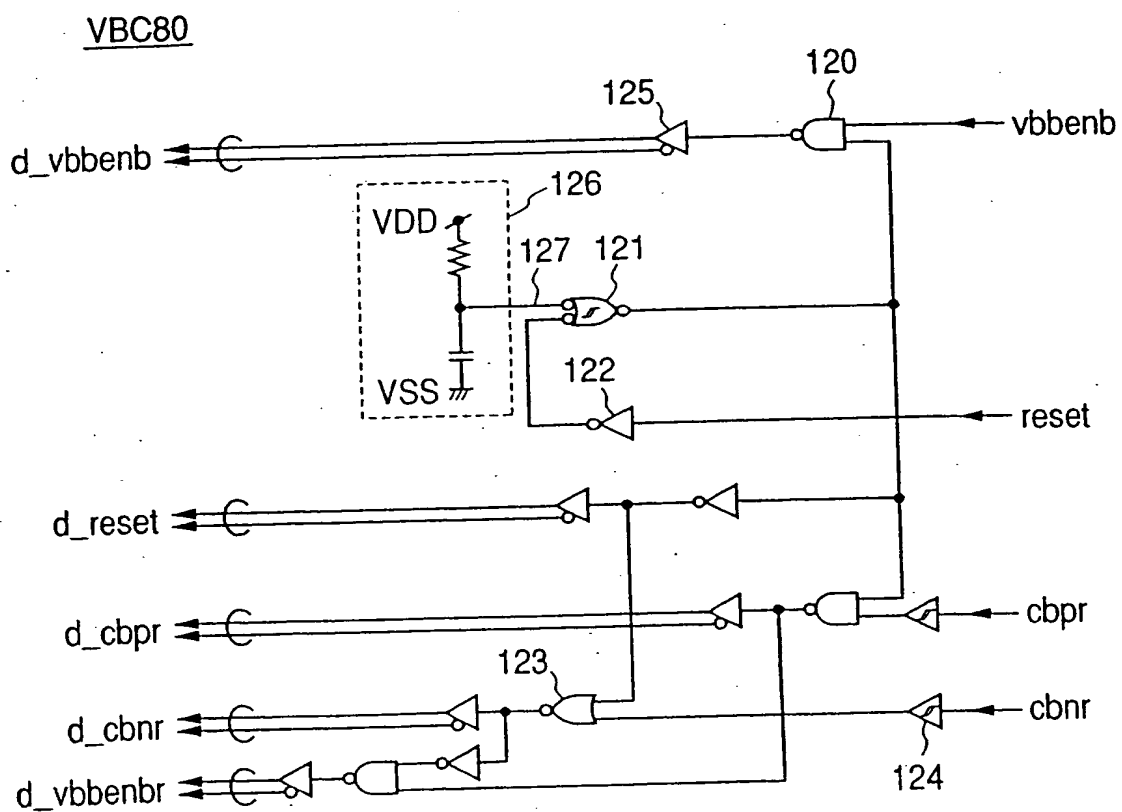


FIG. 8

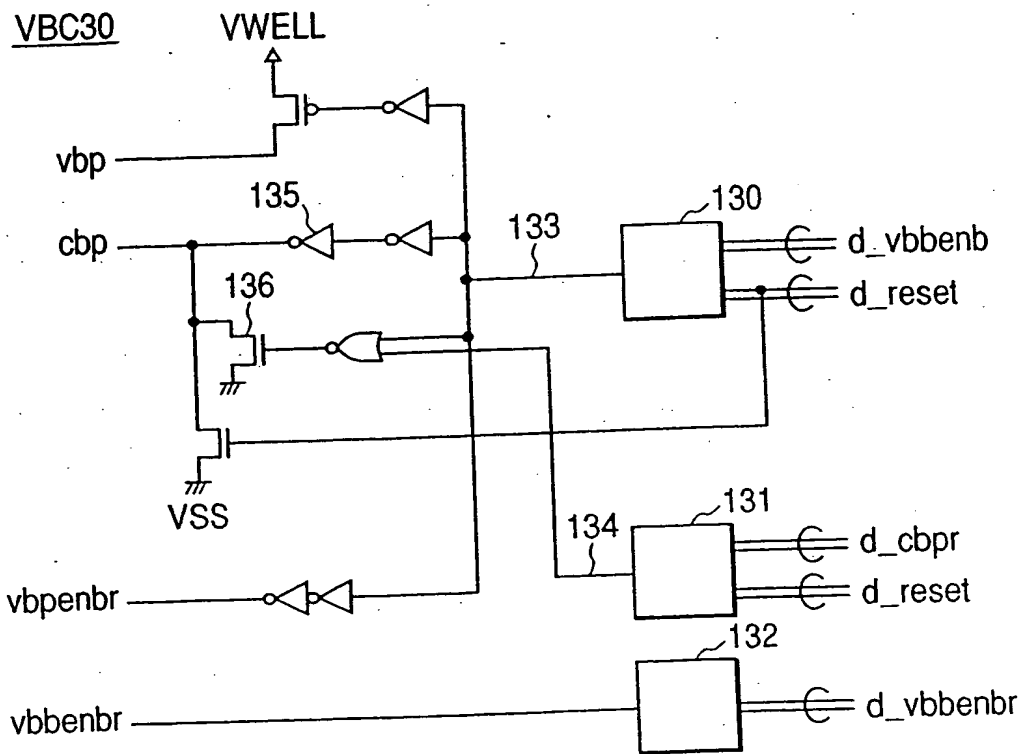


FIG. 9

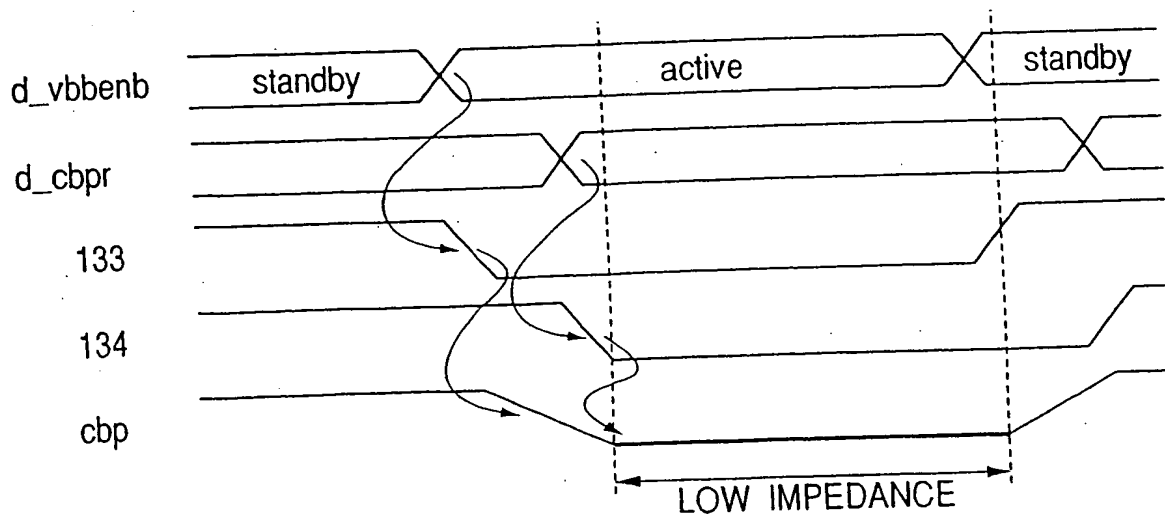


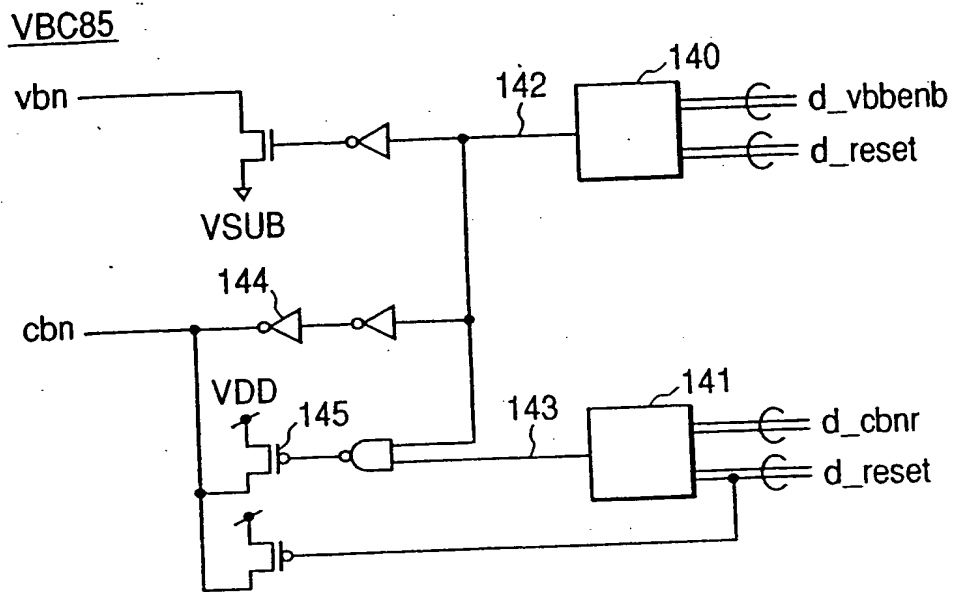
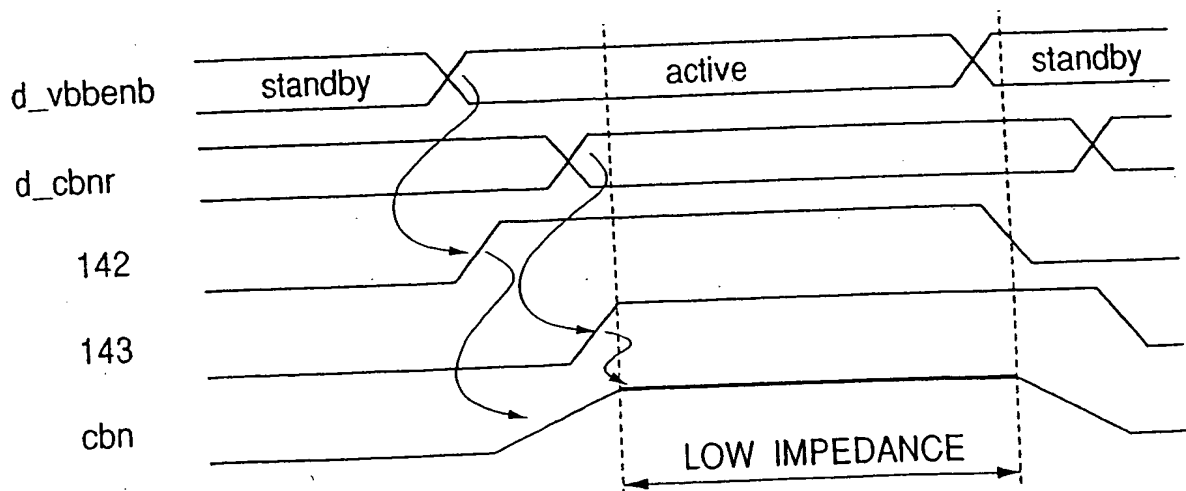
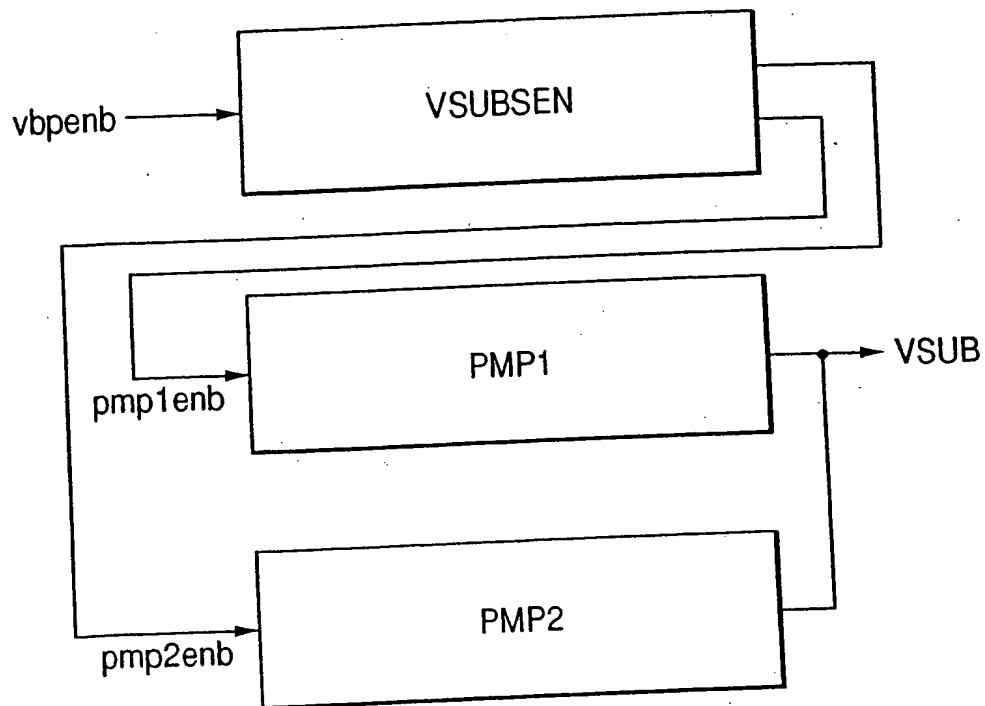
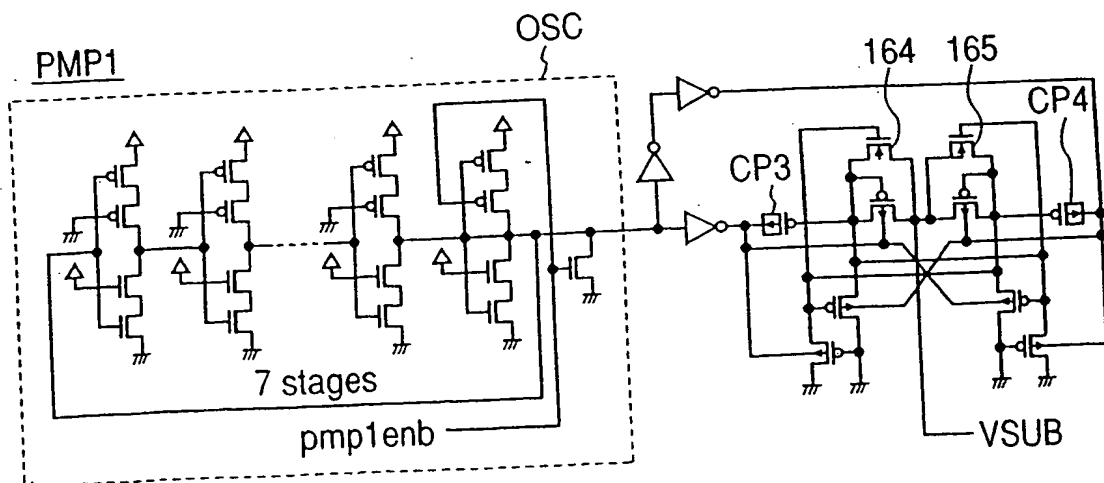
FIG. 10**FIG. 11**

FIG. 12VSUBGEN**FIG. 13**

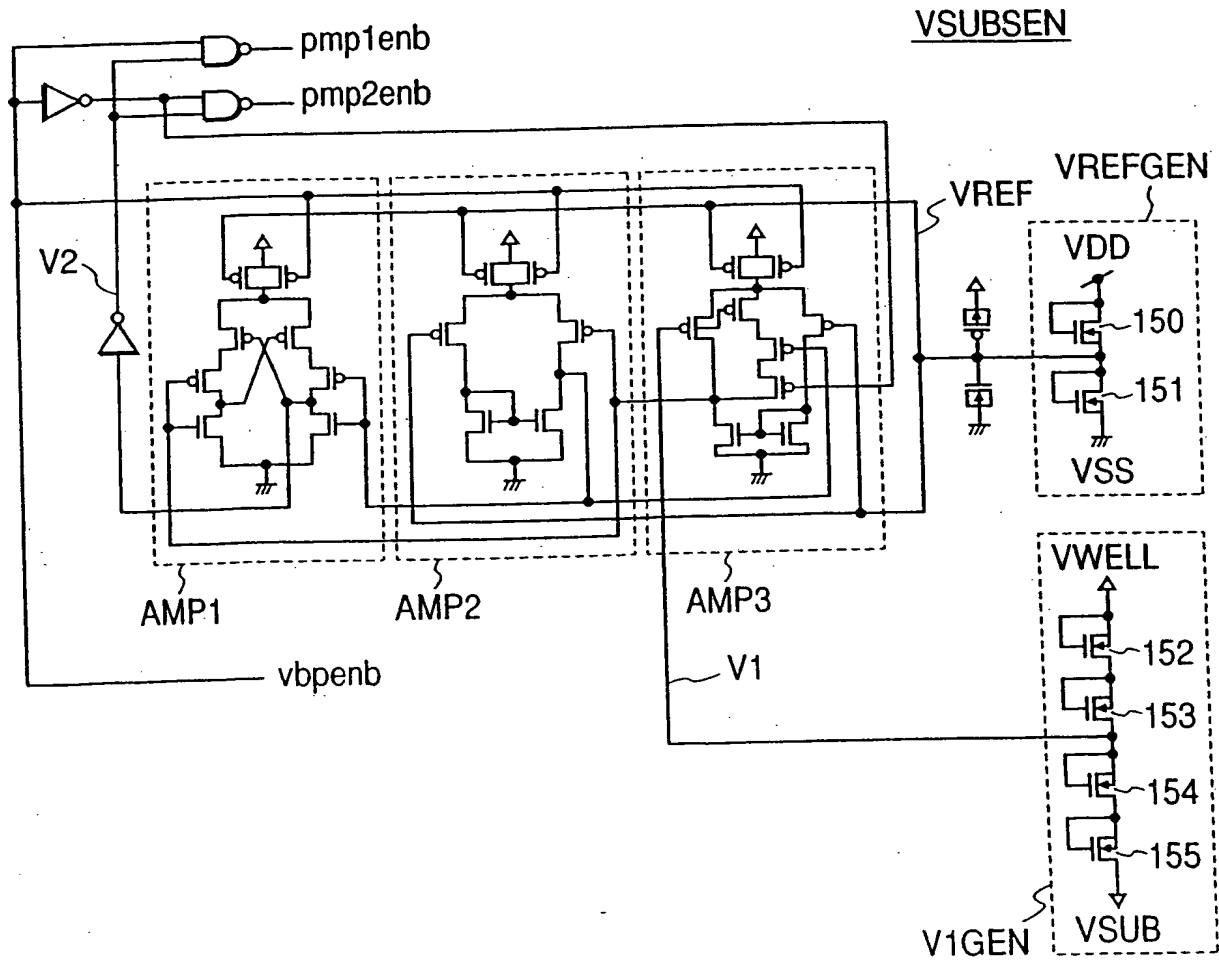


FIG. 16

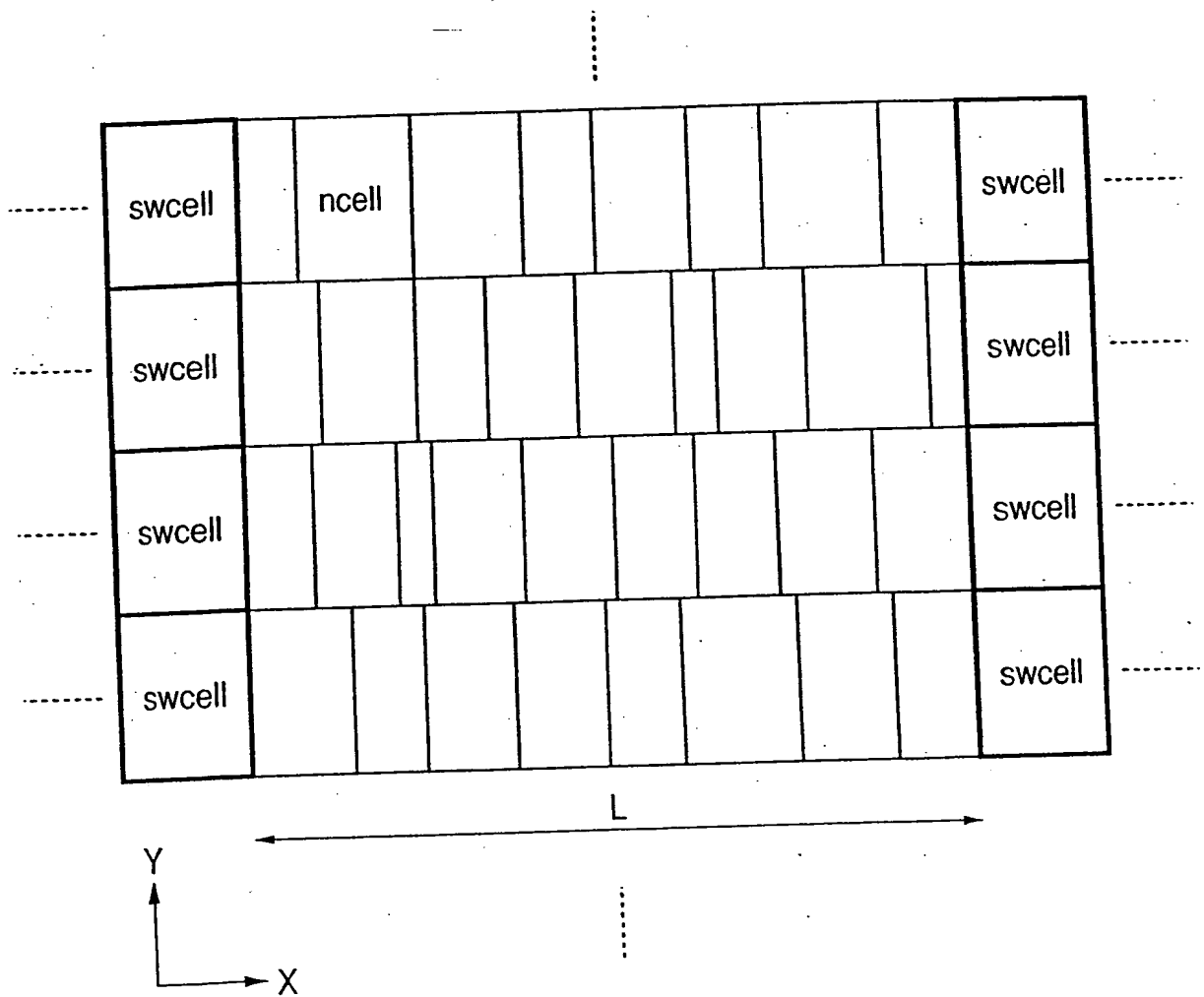
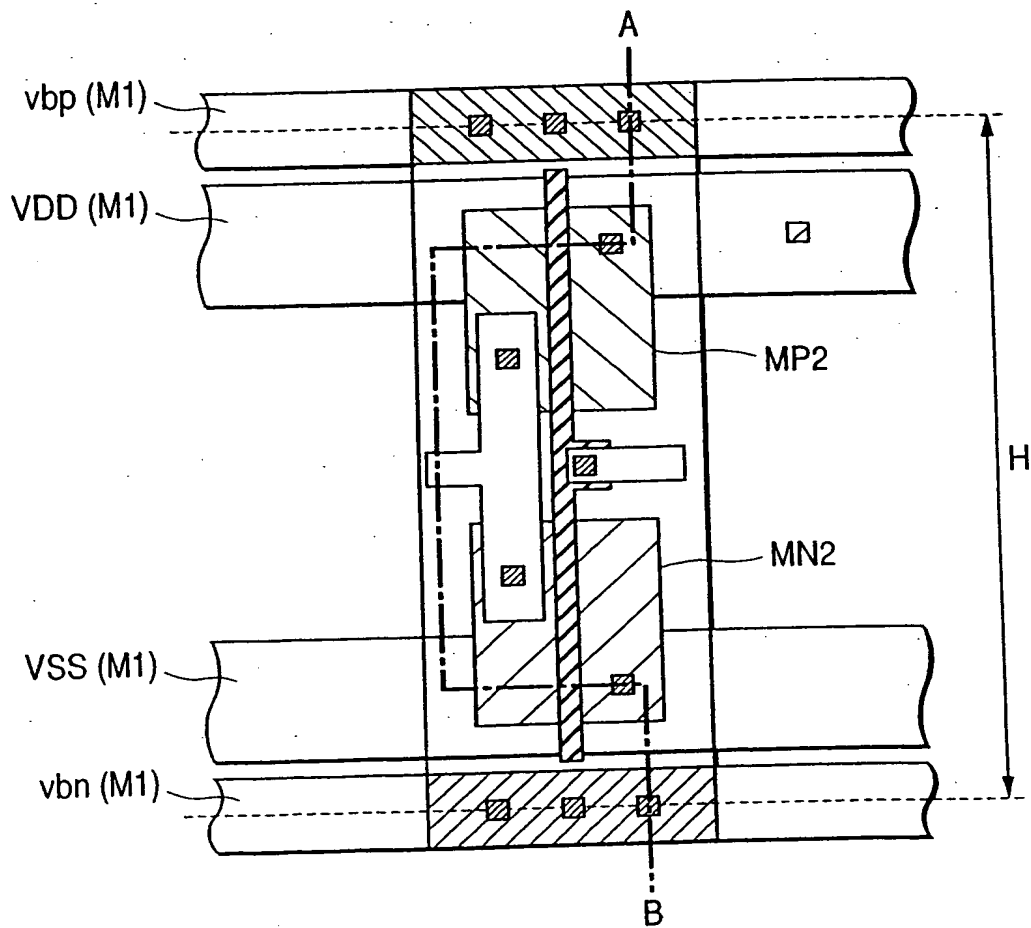


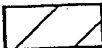
FIG. 17

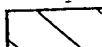


 GATE ELECTRODE

 M1

 CONTACT HOLE

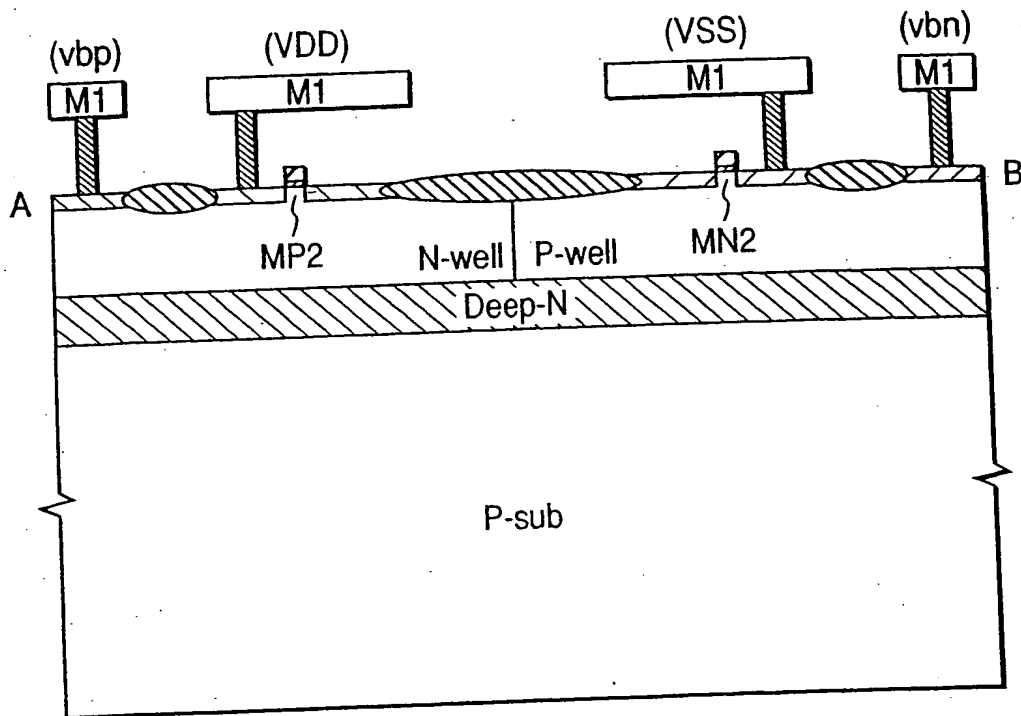
 NMOS ACTIVE AREA


 PMOS ACTIVE AREA


 SURFACE HIGH DENSITY N AREA FOR PMOS V_{BB} SUPPLY

 SURFACE HIGH DENSITY P AREA FOR NMOS V_{BB} SUPPLY


FIG. 18



 GATE OXIDIZATION FILM

 GATE ELECTRODE

 ISOLATION

 M1-M2 VIA HOLE

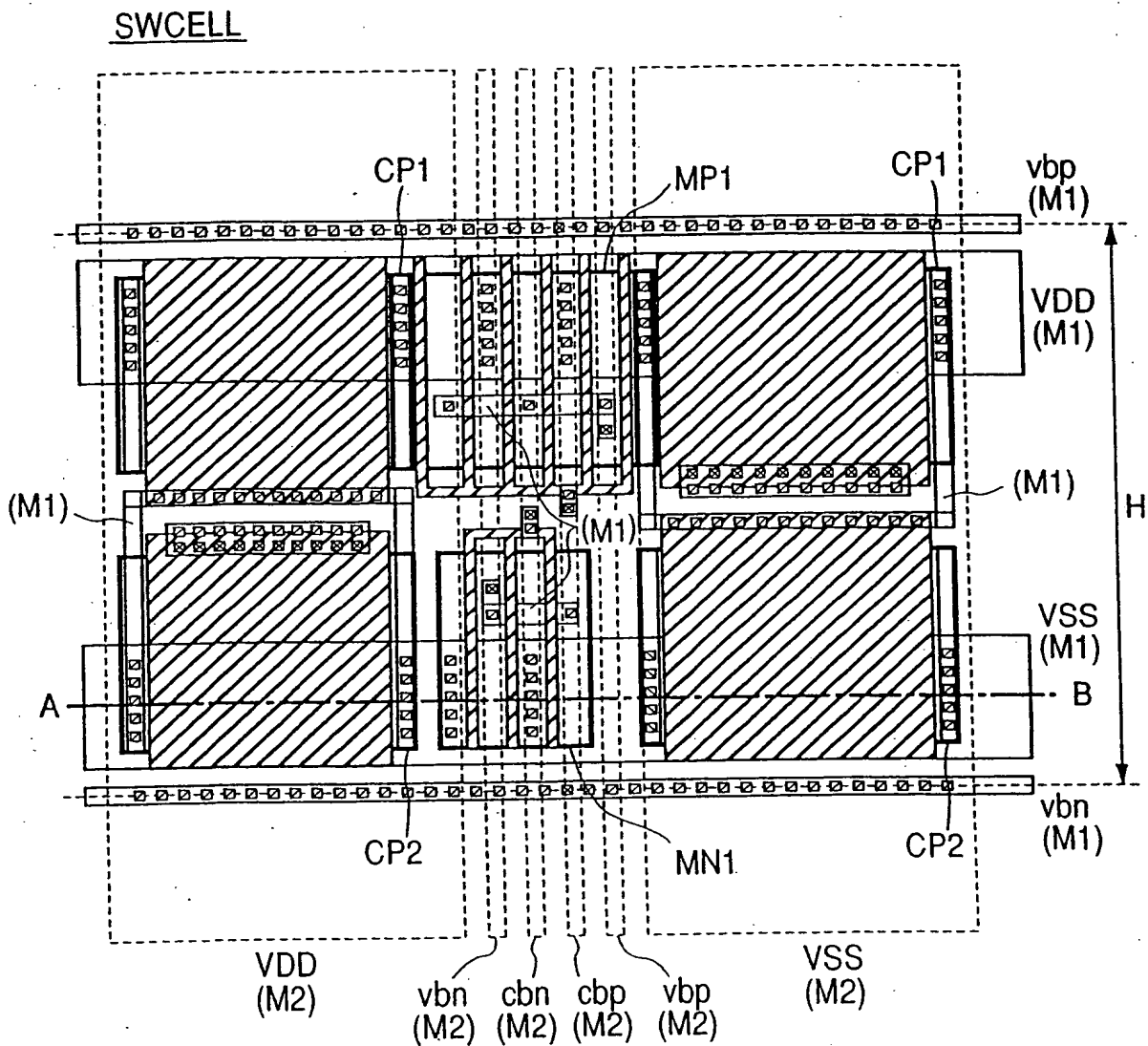
 NMOS ACTIVE AREA (N+)

 PMOS ACTIVE AREA (P+)

 SURFACE HIGH DENSITY N AREA FOR PMOS V_{BB} SUPPLY

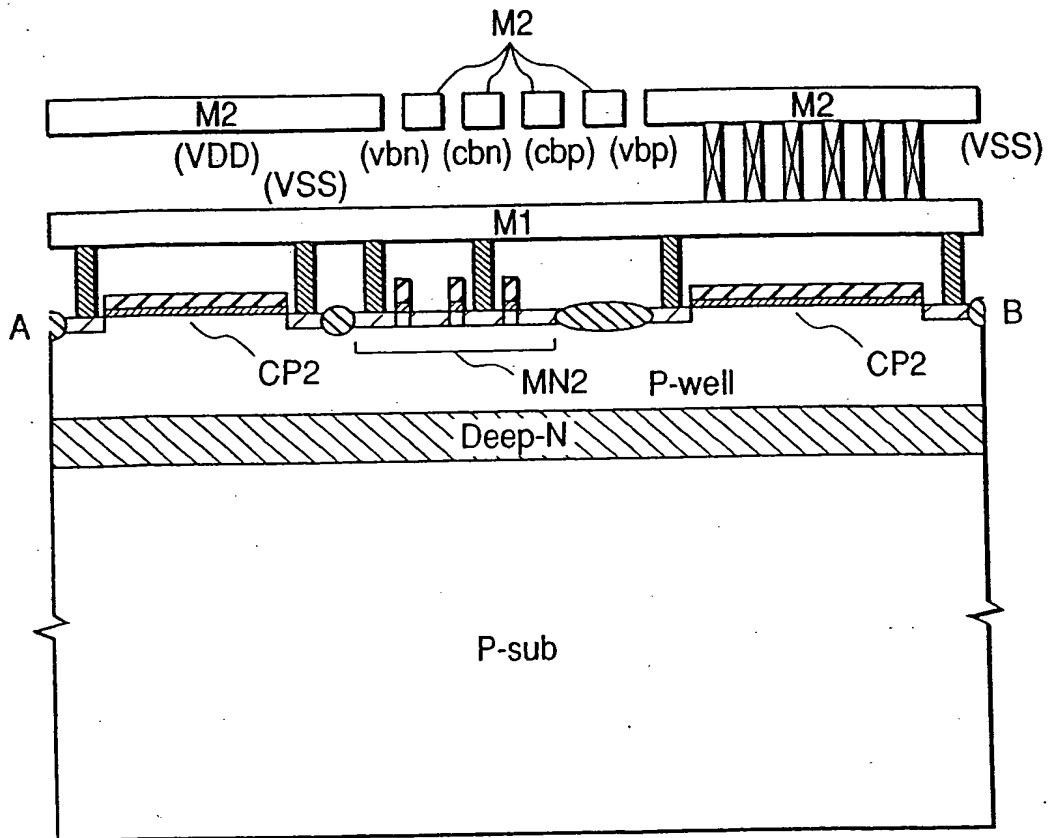
 SURFACE HIGH DENSITY P AREA FOR NMOS V_{BB} SUPPLY

FIG. 19



- | | |
|----------------|-------------|
| GATE ELECTRODE | ACTIVE AREA |
| CONTACT-HOLE | M1 |
| M1-M2 VIA HOLE | M2 |

FIG. 20



M1-M2 VIA HOLE

CONTACT HOLE

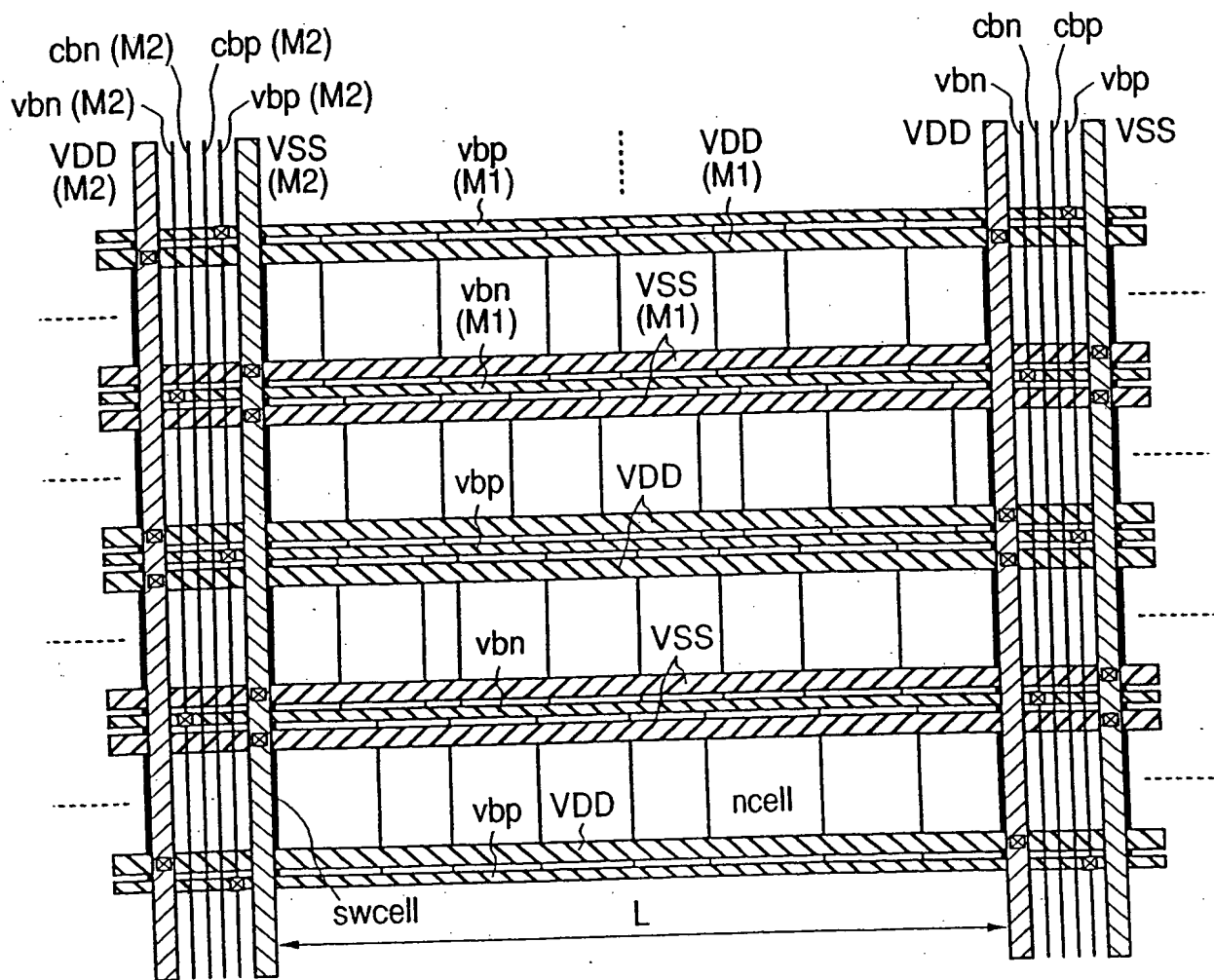
GATE ELECTRODE

GATE OXIDIZATION FILM

ISOLATION

N+ DIFFUSION FILM

FIG. 21



⊠ M1-M2 VIA HOLE

FIG. 22

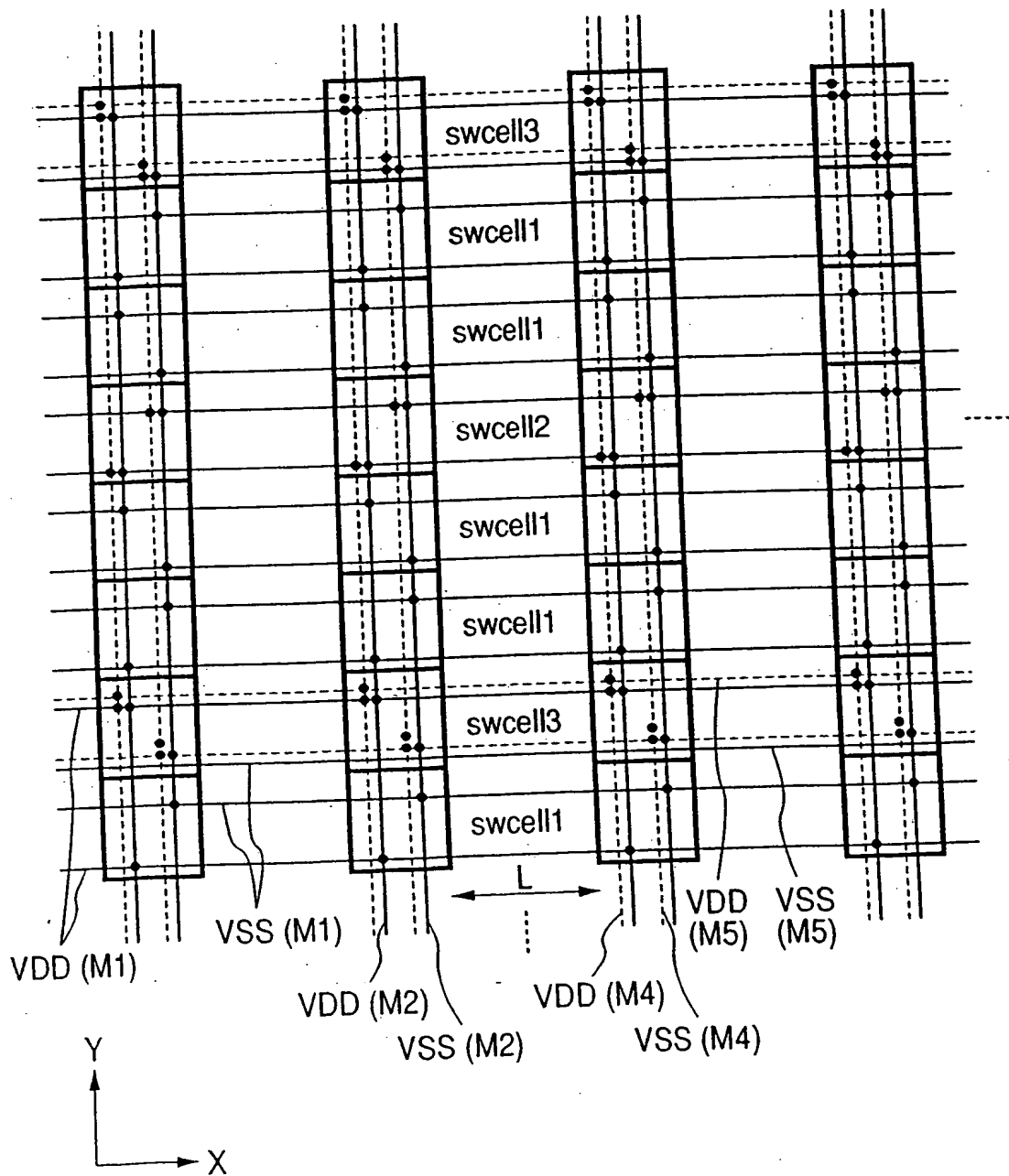


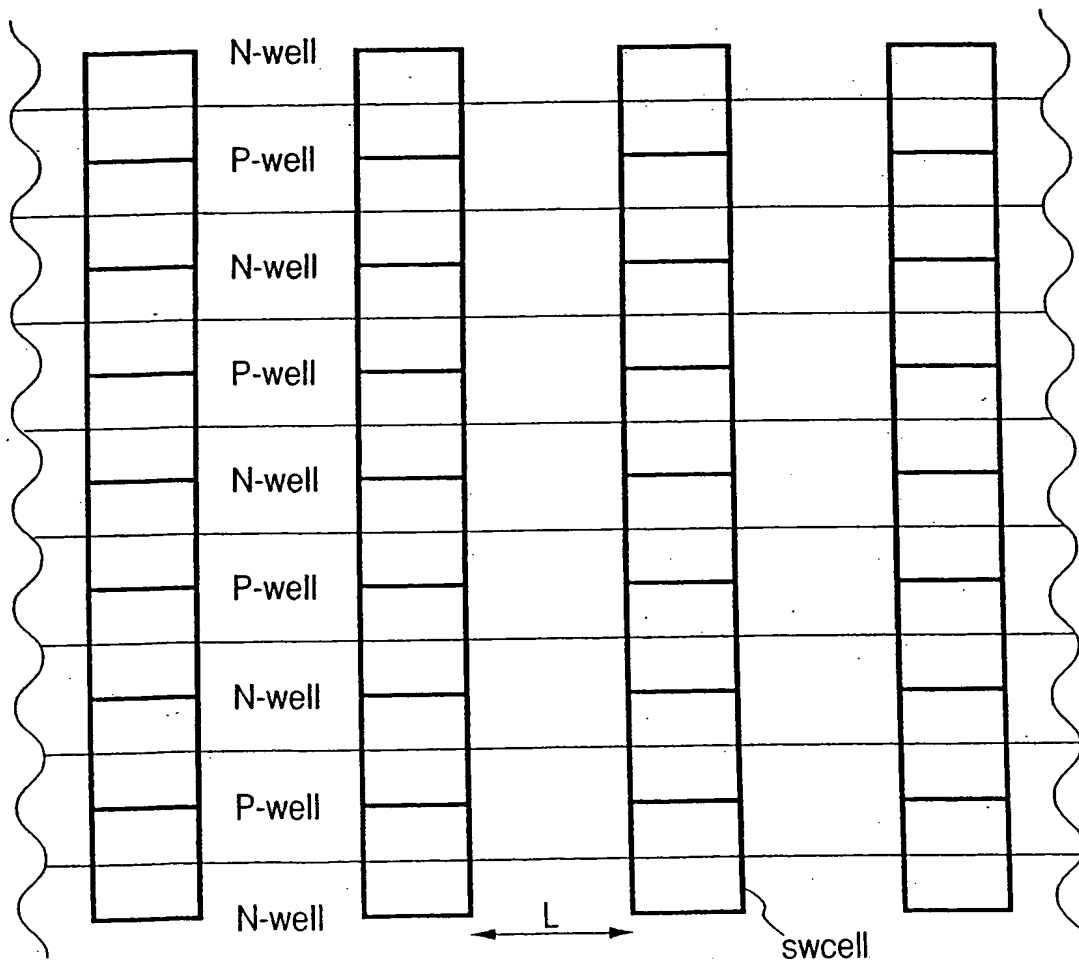
FIG. 23

FIG. 24

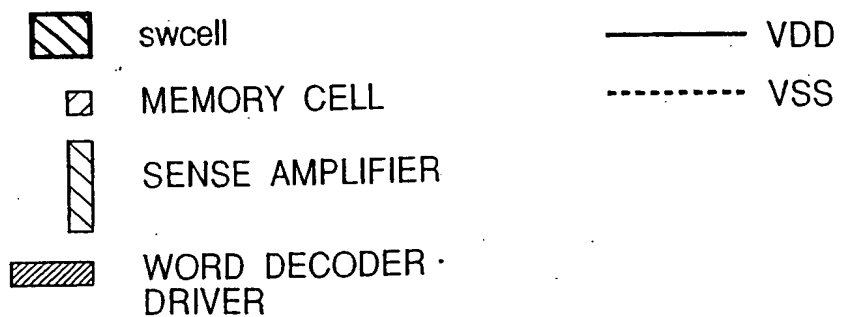
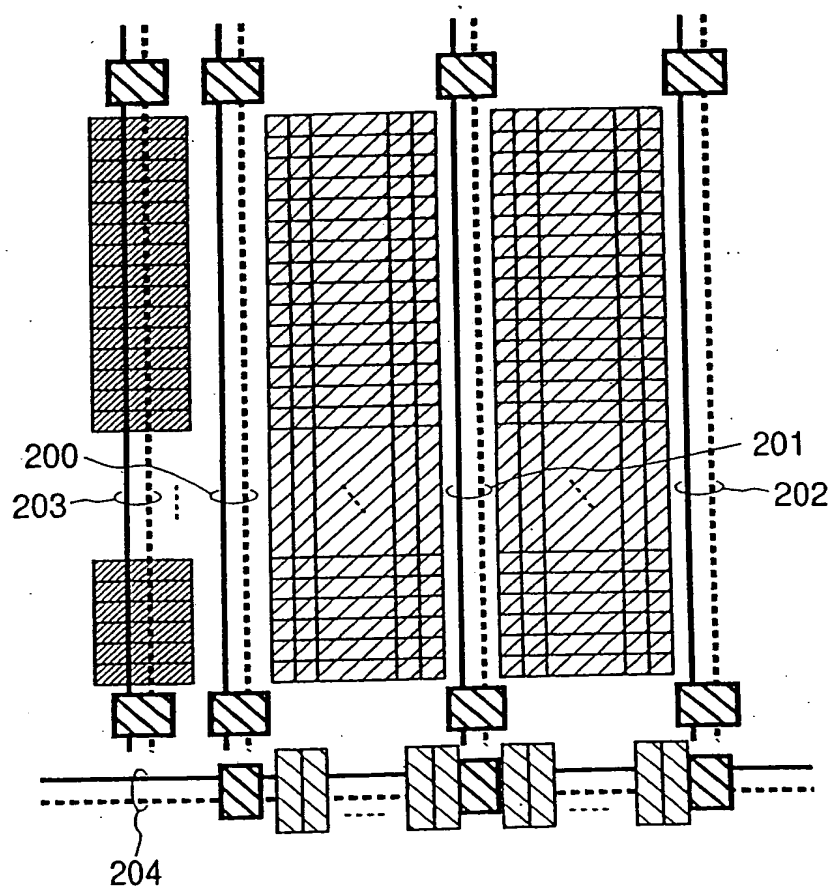


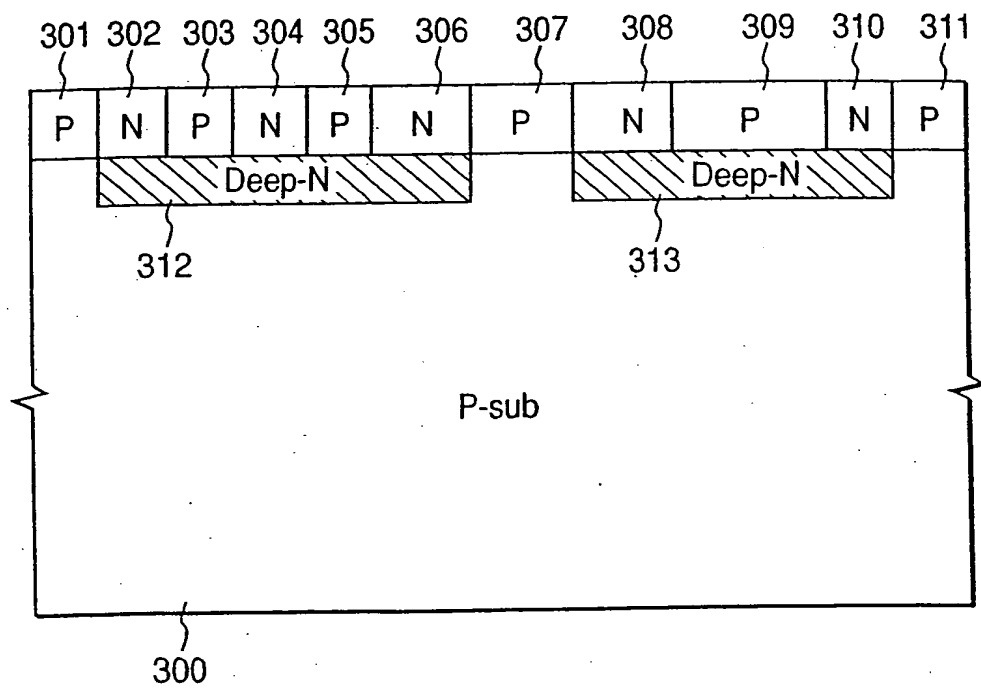
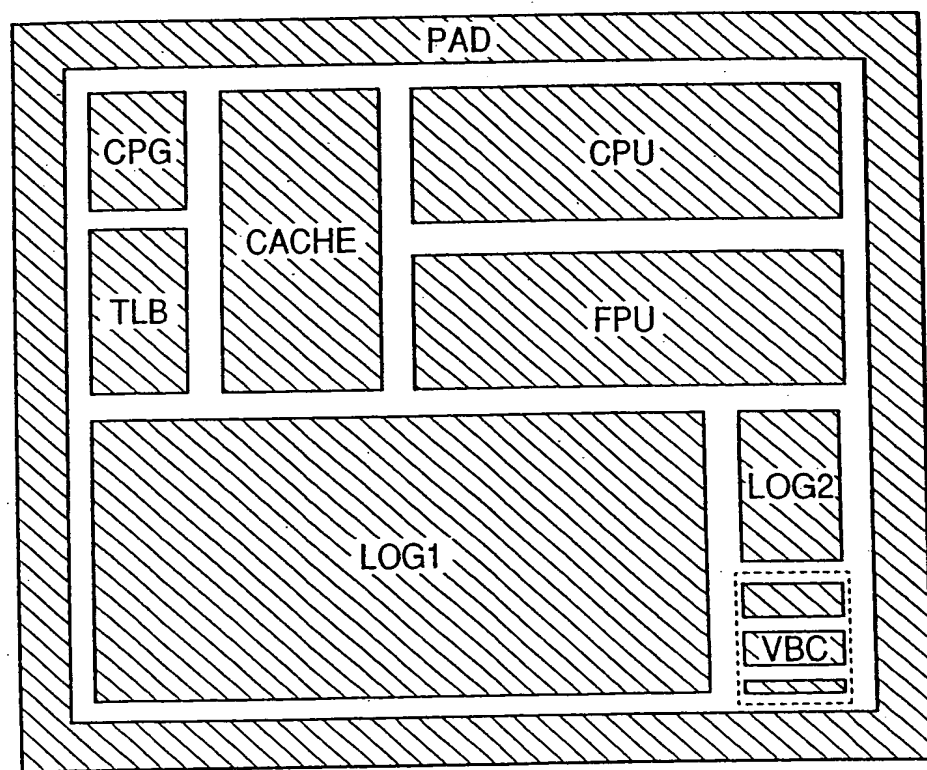
FIG. 25

FIG. 26

 Deep-N

FIG. 27

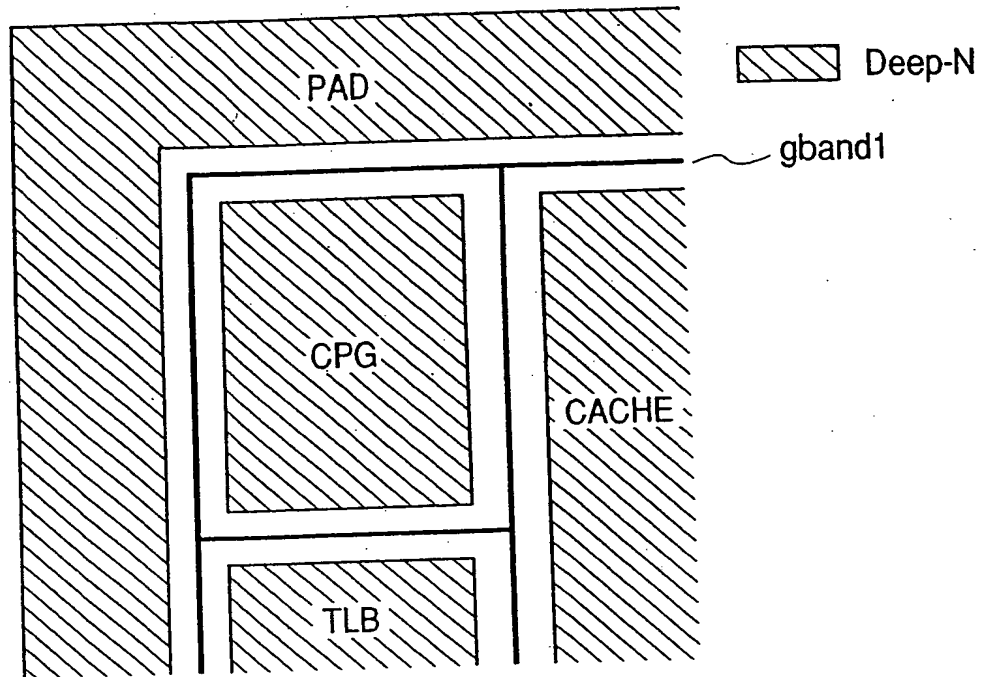


FIG. 28

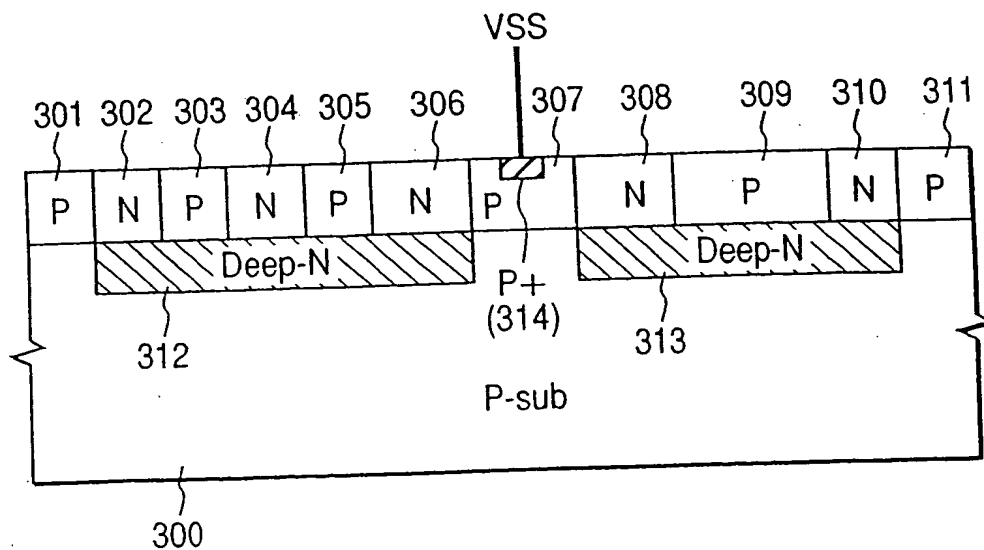


FIG. 29

